International
IOR Rectifier

Data Sheet No. PD 94716

IR3094PBF

3 PHASE PWM CONTROLLER FOR POINT OF LOAD

DESCRIPTION

The IR3094 Control IC provides a full featured, cost effective, single chip solution to offers a compact, efficient solution for high current POL converters. Control and 3 Phase Gate Drive functions are integrated into a single space-saving IC.

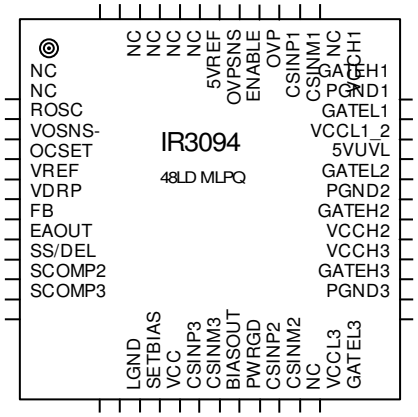
FEATURES

- 0.85V Reference Voltage
- 3A GATELX Pull Down Drive Capability
- Programmable 100KHz to 540KHz oscillator
- Programmable Voltage Positioning (can be disabled)
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Powergood provides indication of proper operation and avoids false triggering
- Operates up to 16V converter input with 7.5V Under-Voltage Lockout
- 4.36V Under-Voltage Lockout threshold for gate driver voltage
- Adjustable Voltage, 150mA Bias Regulator provides MOSFET Drive Voltage
- Enable Input
- OVP Flag Output detects high side fet short at powerup
- Separate OVP sense line to sense the output voltage and latched OVP with protection
- Inductor DCR sensing for current sensing will support up to 5.1V output applications
- Available 48L MLPQ package

ORDERING INFORMATION

Device	Order Quantity
IR3094MTRPBF	3000 per Reel
IR3094MPBF	100 piece strips

PACKAGE INFORMATION



48L MLPQ
(7 x 7 mm Body)
θ_{JA} = 27°C/W

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..0°C to 150°C
Storage Temperature Range…….-65°C to 150°C

PIN	NAME	VMAX	VMIN	ISOURCE	ISINK
3	ROSC	20V	-0.3V	1mA	1mA
4	VOSNS-	0.5V	-0.5V	10mA	1mA
5	OCSET	20V	-0.3V	1mA	1mA
6	VDAC	20V	-0.3V	1mA	1mA
7	VDRP	20V	-0.3V	25mA	5mA
8	FB	20V	-0.3V	1mA	1mA
9	EAOUT	10V	-0.3V	5mA	10mA
10	SS/DEL	20V	-0.3V	1mA	1mA
11	SCOMP2	20V	-0.3V	1mA	1mA
12	SCOMP3	20V	-0.3V	1mA	1mA
13	LGND	n/a	n/a	50mA	1mA
14	SETBIAS	20V	-0.3V	1mA	1mA
15	VCC	20V	-0.3V	1mA	500mA
16	CSINP3	20V	-0.3V	1mA	1mA
17	CSINM3	20V	-0.3V	1mA	1mA
18	BIASOUT	20V	-0.3V	450mA	1mA
19	PWRGD	20V	-0.3V	1mA	20mA
20	CSINP2	20V	-0.3V	1mA	1mA
21	CSINM2	20V	-0.3V	1mA	1mA
22	NC	n/a	n/a	n/a	n/a
23	VCCL3	20V	-0.3V	n/a	3A for 100ns, 200mA DC
24	GATEL3	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
25	PGND3	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
26	GATEH3	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
27	VCCH3	30V	-0.3V	n/a	3A for 100ns, 200mA DC
28	VCCH2	30V	-0.3V	n/a	3A for 100ns, 200mA DC
29	GATEH2	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
30	PGND2	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
31	GATEL2	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
32	5VUVL	20V	-0.3V	1mA	1mA
33	VCCL1_2	20V	-0.3V	n/a	3A for 100ns, 200mA DC
34	GATEL1	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
35	PGND1	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
36	GATEH1	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
37	VCCH1	30V	-0.3V	n/a	3A for 100ns, 200mA DC
38	NC	n/a	n/a	n/a	n/a
39	CSINM1	20V	-0.3V	1mA	1mA
40	CSINP1	20V	-0.3V	1mA	1mA
41	OVP	20V	-0.3V	1mA	1mA
42	ENABLE	20V	-0.3V	1mA	1mA
43	OVPSNS	20V	-0.3V	1mA	1mA
44	5VREF	10V	-0.3V	10mA	20mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 8.0 ≤ V_{CC} ≤ 16V, 4V ≤ V_{CCLX}≤ 14V, 4V ≤ V_{CCHX} ≤ 28V, C_{GATEHX} =3.3nF, C_{GATELX} =6.8nF, 0°C ≤ T_J ≤ 125 °C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VREF Reference					
Sink Current	R_{ROSC} = 47kΩ, VREF=OCSET	45	53	61	μA
Source Current	R_{ROSC} = 47kΩ, VREF=OCSET	48	56	64	μA
System Reference Voltage	Connect FB to EAOUT, Measure V(EAOUT)-V(VOSNS-). Applies to -0.3V<VOSNS-<0.3V.	0.8415	0.85	0.8585	V
Error Amplifier					
Input Offset Voltage	Connect FB to EAOUT, Measure V(EAOUT)-V(VREF). Applies to -0.3V<VOSNS-<0.3V. Note 1	-5	-1	3	mV
UVL FB Bias Current		40	90	150	uA
UVL Head Room		1.2	2	2.5	V
DC Gain	Note 1	90	100	105	dB
Gain-Bandwidth Product	Note 1	4	7		MHz
Slew Rate	Note 1, 50mV FB signal		1.25		V/μs
Source Current		300	430	600	μA
Sink Current		.75	1.1	1.5	mA
Max Voltage		4.5	4.9	5.3	V
Min Voltage			50	200	mV
VDRP Buffer Amplifier					
Positioning Offset Voltage	V(VDRP) – V(REF) with CSINMX=CSINPX=0. Note 1.	-125	0	125	mV
Output Voltage Range		0.2		3.75	V
Source Current		4	8	20	mA
Sink Current		200	300	650	μA
Oscillator					
Switching Frequency	R_{ROSC} = 47kΩ	160	200	240	kHz
Phase Shift	Sequence: GATEH1-GATEH2-GATEH3	102	120	138	°

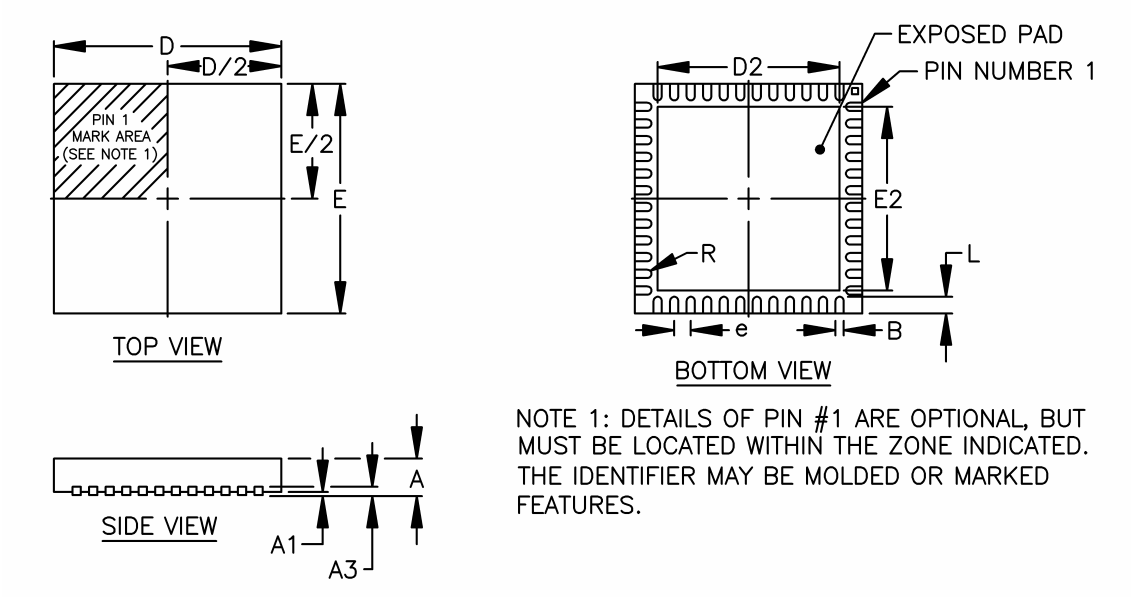
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BIASOUT Regulator					
SETBIAS Bias Current	R_{ROSC} = 47kΩ	94	103	117.5	µA
Set Point Accuracy	V(SETBIAS)-V(BIASOUT) @ 100mA	0	0.25	0.55	V
BIASOUT Dropout Voltage	I(BIASOUT)=100mA,Threshold when V(SETBIAS)-V(BIASOUT)=0.45V	1.2	1.8	2.5	V
BIASOUT Current Limit		150	250	500	mA
Soft Start and Delay					
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.8	1.1	1.8	V
Charge Current		30	60	90	µA
Hiccup Discharge Current		3.5	6	9	µA
OC Discharge Current		25	55	70	µA
Charge/Discharge Current Ratio		9	10	13	µA/µA
Charge Voltage		3.8	4.0	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage	180	245	310	mV
Discharge Comparator Threshold		170	265	350	mV
Over-Current Comparator					
Input Offset Voltage	V(OCSET)-V(VREF), CSINM=CSINP1=CSINP2=CSINP3, Note 1.	-125	0	125	mV
OCSET Bias Current	R_{ROSC} = 47kΩ	23.5	27	29.4	µA
Max OCSET Set Point		3.9			V
Under-Voltage Lockout					
VCC Start Threshold		7.0	7.5	8.0	V
VCC Stop Threshold		6.5	7.0	7.5	V
VCC Hysteresis	Start – Stop	400	500	700	mV
5VUVL Start Threshold		4.05	4.36	4.60	V
5VUVL Stop Threshold		3.92	4.17	4.40	V
5VUVL Hysteresis	Start – Stop	100	200	250	mV
PWRGD Output					
Output Voltage	I(PWRGD) = 4mA		150	400	mV
Leakage Current	V(PWRGD) = 5.5V		0	10	µA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Enable Input					
Threshold	Referenced to VOSNS-	1.3	1.5	1.7	V
Input Resistance		5	10	20	kΩ
Pull-up Voltage		2.4	3.0	3.7	V
Gate Drivers					
GATEH Rise Time	VCCHX = 8V, Measure 1V to 7V transition time. Note 1.		25	50	ns
GATEH Fall Time	VCCHX = 8V, Measure 7V to 1V transition time. Note 1.		25	50	ns
GATEL Rise Time	VCCLX= 8V, Measure 1V to 7V transition time. Note 1.		50	90	ns
GATEL Fall Time	VCCLX= 8V, Measure 7V to 1V transition time. Note 1.		30	60	ns
High Voltage (AC)	Measure VCCLX– GATELX or VCCHX – GATEHX, Note 1		0	0.5V	V
Low Voltage (AC)	Measure GATELX or GATEHX, Note 1		0	0.5V	V
GATEL low to GATEH high delay	VCCHX = VCCLX= 8V, Measure the time from GATELX falling to 1V to GATEHX rising to 1V. Note 1.	10	25	50	ns
GATEH low to GATEL high delay	VCCHX = VCCLX= 8V, Measure the time from GATEHX falling to 1V to GATELX rising to 1V. Note 1.	10	25	50	ns
Disable Pull-Down Current	GATHX or GATELX=2V with VCC = 0V. Measure Gate pull-down current	20	35	50	μA
PWM Comparator					
Propagation Delay	Note1		100	150	ns
Common Mode Input Range				4	V
Internal Ramp Start Voltage		0.44	0.6	0.9	V
Internal Ramp Amplitude		35	50	65	mV / %DTC
Current Sense Amplifier					
CSINPX Bias Current		-1	0	1	μA
CSINM2,3 Bias Current		-1	0	1	μA
CSINM1 Bias Current		-2	-0.5	1	μA
Phase 2 and 3 Input Current Offset Ratio			1		μA/μA
Phase 1 Input Current Offset Ratio		0.5	1.7	4	μA/μA
Average Input Offset Voltage	(VDRP-VREF)/GAIN with CSINX=0. Note1	-5	0	5	mV
Offset Voltage Mismatch	Monitor I(SCOMPX), Note1.	-5	0	5	mV
Gain at T_J = 25 °C		22.5	24	25.5	V/V
Gain at T_J = 125 °C		19	20.9	22	V/V
Gain Mismatch	Note 1.	-1	0	1	V/V
Differential Input Range		-25		75	mV
Common Mode Input Range		-0.2		5.5	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Share Adjust Error Amplifier					
Input Offset Voltage	Note 1	-5	0	5	mV
MAX Duty Cycle Adjust Ratio	Compare Duty Cycle to GATEH1	1.5	2.0		
MIN Duty Cycle Adjust Ratio	Compare Duty Cycle to GATEH1	0.6	0.5		
Transconductance	Note 1	100	200	300	μA/V
SCOMPX Source/Sink Current		16	22	28	μA
SCOMPX Precondition and GATELX Release Threshold	V(FB)	0.6	0.67	0.74	V
SCOMP precondition current		160	360	560	μA
Duty Cycle Match at Startup	Compare Duty Cycle to GATEHX	-7	-1	7	%
0% Duty Cycle Comparator					
Threshold Voltage	Below Internal Ramp1 Start Voltage	-25	25	75	mV
Propagation Delay	VCCLX= 8V. Step EAOUT from .8V to .3V and measure time to GATELX transition to < 7V.		200	400	ns
OVP					
Comparator Threshold	Compare to V(VREF)	120	150	200	mV
Power-up Headroom for OVP Flag	VCC=OVPSNS where V(OVP)>0.5V. Same for 5VUVL=OVPSNS.	0.8	1.1	1.8	V
OVPSNS Threshold at Power-up	VCC=2V, V(OVP) >0.5V. Same for V(5VUVL)=2V.	0.3	0.48	0.85	V
SS/DEL Power-up Clear Threshold	VCC=12V, V(OVPSNS)=1V, VREF=1.6V, where OVP<0.5V	0.35	0.60	0.95	V
Propagation Delay	VCCLX= 8V. V(EAOUT)=0V. Step OVPSNS 540mV + V(VREF). Measure time to GATELX transition to >1V. Note 1.	150	350	650	ns
OVP Source Current	V(OVP)=0.5V, VCC=1.8V, 5VUVL=0V	10	75		μA
OVP Pull Down Resistance	OVP to LGND	30	60	100	kΩ
OVP High Voltage	I(OVP)=10uA, V(VCC) or V(5VUVL)-V(OVP), VCC=1.8V	0.4	0.70	1.1	V
OVPSNS Bias Current		-6.0	-3.0	1.5	uA
5VREF					
Short Circuit Current		20	45	60	mA
Supply Voltage	I(5VREF)=0A	4.5	5	5.5	V
General					
VCC Supply Current	V(VCC)=16V	28.5	35	40.5	mA
VOSNS- Current	-0.3V ≤ VOSNS- ≤ 0.3V	0.6	0.8	1.2	mA
VCCHX and VCCL3 Current	V(VCCHX)=28V, V(VCCL3)=14V	3	5	7	mA
VCCL1_2 Supply Current	V(VCCL1_2)=14V	6	10	17	mA
5VUVL Supply Current	V(5VUVL)=5V, no OVP condition	100	200	400	uA
Non_Sync to Sync Threshold		70.6	77.7	87	%VREF

Note 1: Guaranteed by design, but not tested in production
Note 2: VREF Output is trimmed to compensate for Error Amp input offsets errors

PACKAGE DIMENSIONS



NOTE 1: DETAILS OF PIN #1 ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE IDENTIFIER MAY BE MOLDED OR MARKED FEATURES.

SYMBOL	48–PIN 7X7		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 REF		
B	0.18	0.25	0.30
D	7.00 BSC		
D2	5.50	5.65	5.80
E	7.00 BSC		
E2	5.50	5.65	5.80
e	0.50 BSC		
L	0.35	0.40	0.45
R	0.09	—	—

NOTE: ALL DIMENSIONS ARE IN MILLMETERS.